REMARKS

The Office Action dated August 28, 2003, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

Claims 1, 6, 16 and 21 have been amended. Applicant submits that the amendments made herein are fully supported in the specification and the drawings as originally filed. In particular, support for the amendments appears on page 15, line 4 to page 16, line 6 and in Figs. 6 and 7 of the present specification, and therefore no new matter has been added. Accordingly, claims 1, 2 and 4-21 are pending in the present application and are respectfully submitted for consideration.

Claims 6 and 21 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. In making this rejection, the Examiner took the position that the limitation of "the internal signal having a second phase that is the same as the first phase of the data strobe signal" is not shown in the drawings. Claims 6 and 21 have been amended to more particularly point out and distinctly claim the subject matter of the present invention. Therefore, Applicant submits that the claims are in full compliance with US patent practice, and request that the rejection be withdrawn.

Claims 1, 2, 4, 5 and 16-18 were rejected under 35 U.S.C. § 102(b) as being anticipated by Takahashi et al. (JP 409270700, hereinafter "Takahashi"). Applicant respectfully submits that each of claims 1, 2, 4, 5 and 16-18 recites subject matter that is neither disclosed nor suggested by the cited prior art.

Claim 1 recites an input circuit having a current mirror circuit including a self-biased transistor and a non-self-biased transistor connected to each other, a differential circuit including a first transistor a first drain of which is connected to the non-self-biased transistor for receiving an external signal and a second transistor a second drain of which is connected to the self-biased transistor for receiving a reference signal. The first source of the first transistor and a second source of the second transistor are connected in common and have the same potential, and the differential circuit generates an internal signal at the first drain in accordance with a current flowing through the first and second transistors. In addition, the input circuit includes a constant current source connected to the first source of the first transistor, and a current regulating circuit connected to the second source of the second transistor and connected in parallel to the constant current source. The current regulating circuit increases an amount of the current flowing through the differential circuit in response to the internal signal when the first transistor is turned on, and the current regulating circuit decreases an amount of the current flowing through the differential circuit in response to the internal signal when the first transistor is turned off.

Claim 16 recites an input circuit comprising a first MOS transistor having a gate that receives a data signal, a second MOS transistor having a gate connected to a reference voltage, wherein the source of the first transistor is connected to the source of the second transistor at a first node, a third MOS transistor connected between the first node and a low potential power supply, and having its gate connected to a high potential power supply, a fourth MOS transistor connected between the first node and the low potential power supply, a fifth MOS transistor connected between the drain of

the first transistor and the high potential power supply, a sixth MOS transistor connected between the drain of the second transistor and the high potential power supply, wherein the gates of the fifth and sixth transistors are connected to each other and to the drain of the sixth transistor, and a first inverter haring an input terminal connected to a second node between the first and fifth transistors and an output terminal connected to the gate of the fourth transistor. The fourth MOS transistor is turned on when the first MOS transistor is turned on, and the fourth MOS transistor is turned off when the first MOS transistor is turned off.

Accordingly, at least one of the essential features of the present invention is a current regulating circuit that increases an amount of the current flowing through the differential circuit in response to the internal signal when the first transistor is turned on, and the current regulating circuit decreases an amount of the current flowing through the differential circuit in response to the internal signal when the first transistor is turned off, as recited in claim 1, and an input circuit having a first inverter having an input terminal connected to a second node between the first and fifth transistors and an output terminal connected to the gate of the fourth transistor wherein the fourth MOS transistor is turned on when the first MOS transistor is turned on, and the fourth MOS transistor is turned off when the first MOS transistor is turned off, as recited in claim 16. As such, the present invention results in the advantage of having an input circuit generating internal input signals which rise and fall in response to the rising edges and the falling edges of an external input signal.

It is respectfully submitted that the prior art fails to disclose or suggest the elements of the Applicant's invention as set forth in claims 1, 2, 4, 5 and 16-18, and therefore fails to provide the advantages which are provided by the present application.

Takahashi discloses a transistor (P2 or N6) for receiving an internal signal (i.e., differential output signal) via a three stage inverter (DL1 or DL2).

Applicant respectfully submits that each and every element recited within claims 1 and 16 is neither disclosed nor suggested by Takahashi. In particular, Applicant submits that the input circuit as recited in the present application is clearly distinct from that which is illustrated by the combination of the cited prior art. Specifically, it is submitted that the cited prior art fails to disclose or suggest at least the limitation "wherein the current regulating circuit increases an amount of the current flowing through the differential circuit in response to the internal signal when the first transistor is turned on, and the current regulating circuit decreases an amount of the current flowing through the differential circuit in response to the internal signal when the first transistor is turned off", and "a first inverter having an input terminal connected to a second node between the first and fifth transistors and an output terminal connected to the gate of the fourth transistor wherein the fourth MOS transistor is turned on when the first MOS transistor is turned on, and the fourth MOS transistor is turned off when the first MOS transistor is turned off."

It is submitted that Takahashi fails to disclose or suggest that a transistor which increases an amount of current flowing through the differential circuit when a transistor is turned on and decreases an amount of the current when the transistor is turned off. In contrast, Takahashi discloses that when the transistor (P3 or N3) is turned on, the

transistor (P2 or N6) is turned off, and when the transistor (P3 or N3) is turned off, the transistor (P2 or N6) is turned on. Applicant submits that Takahashi discloses subject matter that is completely contrary to the present invention.

Furthermore, Applicant submits that Fig. 1 of Takahashi merely discloses a first MOS transistor (P3), a second MOS transistor (P4), a third MOS transistor (P1), a fourth MOS transistor (P2), a fifth MOS transistor (N1), a sixth MOS transistor (N2), and a first inverter (V1) having an input terminal connected to a node between the first and fifth transistors (P3, N1) and an output terminal connected to a delay circuit (DL1) and a second inverter (V2). However, it is submitted that Takahashi does not teach or suggest that the fourth MOS transistor (P2) is turned on when the first MOS transistor (P3) is turned on and the fourth MOS transistor (P2) is turned off when the first MOS transistor is turned off (P3). In other words, the fourth MOS transistor (P2) of Takahashi is turned on when the first MOS transistor (P3) is turned off and the fourth MOS transistor (P2) is turned off when the first MOS transistor is turned on (P3), which is contrary to the present invention.

Accordingly, Applicant submits that Takahashi fails to disclose or suggest each and every element recited in claims 1 and 16 of the present application, and therefore claims 1 and 16 is allowable.

As for claims 2, 4, 5, 17 and 18, it is submitted that each of claims 2, 4, 5, 17 and 18 is dependent on independent claims 1 and 16, respectively. As such, each of claims 2, 4, 5, 17 and 18 is allowable due to its dependency on allowable claims 1 and 16, respectively.

Claims 1, 2 and 4-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Figure 1 of the applicant's admitted prior art ("APA") in view of Takahashi. Applicant respectfully submits that each of claims 1, 2 and 4-21 recites subject matter that is neither disclosed nor suggested by the cited prior art.

Claim 6 recites a semiconductor integrated circuit having a plurality of input circuits. Each input circuit includes a differential circuit including a first transistor for receiving an external signal and a second transistor for receiving a reference signal, wherein sources of the first and second transistors are connected in common, and the differential circuit generates an internal signal in accordance with a current flowing through the first and second transistors, and a current regulating circuit, connected to the differential circuit, which increases the amount of the current flowing through the differential circuit in response to the internal signal when the first transistor is turned on, wherein the current regulating circuit decreases the amount of the current flowing through the differential circuit in response to the internal signal when the first transistor is turned off, a plurality of complementary signal generating circuits, each connected to one of the input circuits, wherein the complementary signal generating circuits receive the internal signal from the associated input circuit and generate a complementary signal of the input signal, and a plurality of signal processing circuits connected to the plurality of complementary signal generating circuits, respectively, wherein the signal processing circuits perform predetermined signal processing operations in accordance with the complementary signal.

Claim 21 recites a semiconductor integrated circuit for receiving a data signal in response to rising and falling edges of a data strobe signal having a data strobe signal

input circuit which receives the data strobe signal. The data strobe signal input circuit includes a differential circuit having a first transistor and a second transistor to generate a differential output signal having a logic level, a first gate of the first transistor receiving the data strobe signal, a second gate of the second transistor receiving a reference signal, and sources of the first and second transistor being connected in common and having the same potential, a current mirror circuit supplying a current to the differential circuit, a constant current source coupled to the sources of the first and second transistors, and a current adjustment transistor coupled to the sources of the first and second transistors, a third gate of the current adjustment transistor receiving the differential output signal of the differential circuit, wherein the current adjustment transistor is turned on in response to the logic level of the differential output signal when the first transistor turns on, and the current adjustment transistor is turned off in response to the logic level of the differential output signal when the first transistor is turned off such that a falling delay time and a rising delay time of the logic level of the differential output signal are substantially the same.

The Applicant respectfully submits that each element recited within claims 1, 6, 16 and 21 is neither disclosed nor suggested by APA and/or Takahashi, taking alone or in combination. In particular, it is submitted that APA fails to disclose at least the feature of a current regulating circuit, as claimed in claim 1. Furthermore and as commented above, Takahashi fails to cure the deficient limitation as discussed above. Accordingly, Applicant respectfully submits that claim 1 recites subject matter that is neither disclosed nor suggested in APA and/or Takahashi, taken alone or in combination, and therefore claim 1 is allowable over the cited prior art.

As for the rejection of claim 6, It is submitted that both APA and Takahashi fail to disclose or suggest that a transistor which increases an amount of current flowing through the differential circuit when a transistor is turned on and decreases an amount of the current when the transistor is turned off. In contrast, Takahashi discloses that when the transistor (P3 or N3) is turned on, the transistor (P2 or N6) is turned off, and when the transistor (P3 or N3) is turned off, the transistor (P2 or N6) is turned on. Applicant submits that Takahashi discloses subject matter that is completely contrary to the present invention, and APA fails to cure the deficient limitation in Takahashi. As such, Applicant respectfully submits that claim 6, as amended, therefore recites subject matter that is neither disclosed nor suggested in APA and/or Takahashi, take alone or in combination, and claim 6 is therefore allowable over the cited prior art.

With respect to claim 16, it is submitted that Takahashi merely discloses a first MOS transistor (P3), a second MOS transistor (P4), a third MOS transistor (P1), a fourth MOS transistor (P2), a fifth MOS transistor (N1), a sixth MOS transistor (N2), and a first inverter (V1) having an input terminal connected to a node between the first and fifth transistors (P3, N1) and an output terminal connected to a delay circuit (DL1) and a second inverter (V2). However, Takahashi does not teach or suggest that the fourth MOS transistor (P2) is turned on when the first MOS transistor (P3) is turned on and the fourth MOS transistor (P2) is turned off when the first MOS transistor is turned off (P3). In other words, the fourth MOS transistor (P2) of Takahashi is turned on when the first MOS transistor (P3) is turned off and the fourth MOS transistor (P2) is turned off when the first MOS transistor is turned on (P3), which is contrary to the present invention. Also, it is submitted that APA fails to cure the deficient limitation in Takahashi.

Therefore, Applicant respectfully submits that claim 16, therefore, recites subject matter that is neither disclosed nor suggested in APA and/or Takahashi, taken alone or in combination, and therefore claim 16 is allowable over the cited prior art.

As for claim 21, it is submitted that APA does not disclose a current regulating circuit. As discussed above with respect to claims 1 and 6, Takahashi fails to disclose or suggest that the current adjustment transistor is turned on in response to the logic level of the differential output signal when the first transistor turns on and the current adjustment transistor is turned off in response to the logic level of the differential output signal when the first transistor is turned off. Accordingly, Applicant respectfully submits that claim 21 recites subject matter that is neither disclosed nor suggested in APA and/or Takahashi, taken alone or in combination, and therefore claim 21 is allowable over the cited prior art.

As for claims 2, 4, 5, 7-15, 17-20, it is submitted that each of claims 2, 4, 5, 7-15, 17-20 is dependent on independent claims 1, 6 and 16, respectively. As such, each of claims 2, 4, 5, 7-15, 17-20 is allowable due to its dependency on allowable claims 1, 6 and 16, respectively.

In view of the above, Applicant respectfully submits that each of claims 1, 2 and 4-21 recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicant also submits that this subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore, respectfully requests that claims 1, 2 and 4-21 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the

Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, **referencing docket number 108075-09014.**

Respectfully submitted,

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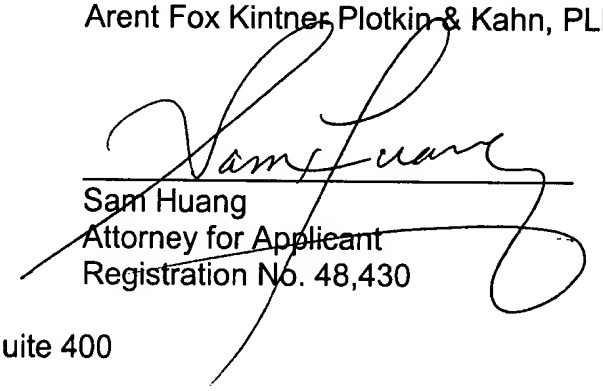

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